IN THE SPECIFICATION

Please amend the specification as follows:

1. Amend paragraph [0084] as follows:

FIG. 1A is a configuration diagram of a signal line connection between a first semiconductor chip and a second semiconductor chip in the semiconductor device according to an embodiment of the present invention;

2. Add the following paragraph between paragraphs [0084] and [0085]:

FIG. 1B illustrates the first semiconductor chip and the second semiconductor chip bonded together such that the chip surfaces face each other;

3. Amend paragraph [0091] as follows:

FIG. 1A is a configuration diagram of a signal line connection between a first semiconductor chip and a second semiconductor chip in a semiconductor device according to an embodiment of the present invention. FIG. 1B illustrates the first semiconductor chip and the second semiconductor chip bonded together such that the chip surfaces face each other. In FIGs. 1A and 1B, 1 indicates the first semiconductor chip, 2 indicates

the second semiconductor chip, 3 indicates a memory macro control circuit formed on first semiconductor chip 1, 4 indicates a first operation mode setting circuit formed on first semiconductor chip 1, 5 indicates a memory macro formed on second semiconductor chip 2, 6 indicates a second operation mode setting circuit formed on second semiconductor chip 2, M1 indicates a first multiplexer circuit, M2 indicates a second multiplexer circuit, M3 indicates a third multiplexer circuit, M4 indicates a fourth multiplexer circuit, D1 indicates a first demultiplexer circuit, D2 indicates a second demultiplexer circuit, D3 indicates a third demultiplexer circuit, D4 indicates a fourth demultiplexer circuit, P1 indicates an external connection terminal connected to an input signal line of first multiplexer circuit M1, P2 indicates an external connection terminal connected to an output signal line of second demultiplexer circuit D2, P3 indicates an external connection terminal connected to an output signal line of first demultiplexer circuit D1, P4 indicates an external connection terminal connected to an input signal line of second demultiplexer circuit M2, P5 indicates an external connection terminal connected to an input signal line of fourth multiplexer circuit M4, P6 indicates an external connection terminal connected to an output signal line of fourth demultiplexer circuit D4, C1 indicates an inter-chip connection terminal

connected to an output signal line of first multiplexer circuit M1, C2 indicates an inter-chip connection terminal connected to an input signal line of first demultiplexer circuit D1, C3 indicates an inter-chip connection terminal connected to an input signal line of third demultiplexer circuit D3, C4 indicates an inter-chip connection terminal connected to an output signal line of third multiplexer circuit M3, S1 indicates a first operation mode setting signal generated by first operation mode setting circuit 4, S2 indicates a second operation mode setting signal generated by first operation mode setting circuit 4, S3 indicates a third operation mode setting signal generated by second operation mode setting circuit 6, S4 indicates a fourth operation mode setting signal generated by second operation mode setting circuit 6, Out1 indicates an output terminal of memory macro control circuit 3, In2 indicates an input terminal of memory macro control circuit 3, In1N indicates an input terminal at the time of the normal operation mode of memory macro 5, In1T indicates an input terminal at the time of the test mode of memory macro 5, Out2N indicates an output terminal at the time of the normal operation mode of memory macro 5, and Out2T indicates an output terminal at the time of the test mode of memory macro 5.